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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,436	04/16/2004	Kosuke Inoue	500.39252VX1	8009

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EXAMINER	
OWENS, DOUGLAS W	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,436	INOUE ET AL.	
	Examiner	Art Unit	
	Douglas W Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,4-10,12-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 April 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/698,186.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/16/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the transistor portion placed in an outer circumferential portion of the semiconductor element, as cited in claims 3 and 11 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 5, 8, 9, 12, 14, 15, 18 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,313,532 to Shimoishizaka et al.

Regarding claim 1, Shimoishizaka et al. teach a semiconductor device comprising:

a semiconductor element (Col. 5, lines 62 – 65);

an external connection terminal (41) connected electrically to the semiconductor element which has at least one electrode (a transistor has at least one electrode); and

an electrically insulating layer (20) between the semiconductor element and the external connection terminal,

wherein the electrically insulating layer has a thickness in a range of 10 to 150 micrometers (Col. 7, lines 4 – 9), which includes the range of 35 to 150 micrometers.

Regarding claim 2, Shimoishizaka et al. teach a device, wherein the semiconductor element includes a transistor portion (Col. 5, lines 62 – 65), and the electrically insulating layer is provided to cover the transistor portion.

Regarding claims 5 and 9, Shimoishizaka et al. teach a device, wherein the external connection terminal is a solder bump (Col. 9, lines 29 – 37).

Regarding claim 8, Shimoishizaka et al. teach a device,

wherein the semiconductor element includes a transistor portion, and

wherein a thickness of a portion of the electrically insulating layer covering the transistor portion of the semiconductor element is greater than a thickness of another portion of the electrically insulating layer covering a different portion of the semiconductor element.

Regarding claim 12, Shimoishizaka et al. teach a device, wherein the external connection terminal is a solder bump, the solder bump inherently has a thickness determined by its location relative to the different thicknesses of the electrically insulating layer, since the layer and bump are identical to that of the claimed invention.

Regarding claim 14, Shimoishizaka et al. teach a semiconductor device comprising:

a semiconductor element (Col. 5, lines 62 – 65);

an external connection terminal (41) connected electrically to the semiconductor element which has at least one electrode (a transistor has at least one electrode);

wherein the semiconductor element includes a transistor portion (Col. 5, lines 62 – 65); and

an electrically insulating layer (20) between the semiconductor element and the external connection terminal,

wherein the electrically insulating layer has a thickness in a range of 10 to 150 micrometers (Col. 7, lines 4 – 9), which includes the range of 35 to 150 micrometers.

Regarding claims 15 and 19, Shimoishizaka et al. teach a semiconductor device, wherein the external connection is a solder bump. With respect to the requirement that the insulating layer intercepts an α-ray generated from the solder bump, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Danly*, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device is, not what a device does." *Hewlett- Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). Accordingly, this limitation has not been given patentable weight.

Regarding claim 18, Shimoishizaka et al. teach a semiconductor device comprising:

a semiconductor element (Col. 5, lines 62 – 65);

an external connection terminal (41) connected electrically to the semiconductor element which has at least one electrode (a transistor has at least one electrode);

wherein the semiconductor element includes a transistor portion (Col. 5, lines 62 – 65); and

an electrically insulating layer (20) between the semiconductor element and the external connection terminal to cover at least the transistor portion, and

wherein the electrically insulating layer has a thickness in a range of 10 to 150 micrometers (Col. 7, lines 4 – 9), which includes the range of 35 to 150 micrometers.

The preamble of the claim merely recites the intended use and has not been given any patentable weight.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoishizaka et al. as applied to claims 1 and 8, and further in view of US Patent No. 6,057,598 to Payne et al.

Shimoishizaka et al. do not teach a device including a memory cell, and wherein the electrically insulating layer covers the memory cell. Payne et al. teach a package structure (200) including a memory cell (202). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a memory cell into the package device taught by Shimoishizaka et al., since the package is perfectly suited for the purpose of packaging memory cells. It is further obvious that the insulating layer would have covered the memory cell, since a memory circuit consists of many memory cells.

6. Claims 6, 7, 10, 13, 16, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoishizaka et al. as applied to claims 1, 2, 5, 8, 9, 12, 14 and 18 above, and further in view of US Patent Application Publication No. 2002/0024124 to Hashimoto.

Shimoishizaka et al. teach a device, wherein the electrically insulating layer has a low elasticity with a modulus in the range of 10 to 2000 kg/mm^2 (Col. 7, lines 4 – 12). Shimoishizaka et al. do not teach a semiconductor device, wherein the electrically insulating layer is a polyimide material. Hashimoto teaches a polyimide having a low elasticity (paragraph [0128]). It would have been obvious to one having ordinary skill in the art to incorporate the low elasticity insulating layer into the device taught by Shimoishizaka et al., since it is desirable to use materials that are well suited for the intended use.

7. Claims 3 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas W. Owens
Patent Examiner